

A1
formed in one of the plurality of element regions and a gate electrode having a first gate length, a second transistor formed in a memory cell portion of the semiconductor substrate, the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length; a contact connected to the one of the source and drain diffusion layers; and a first insulating film different from a silicon oxide covering the second transistor and not covering the first transistor, the first insulating film being an etching stopper for the contact to the element isolation region and having a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.

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Please delete the paragraph beginning on page 5, line 24.

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Please delete the paragraph beginning on page 6, line 2.

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Please delete the paragraph beginning on page 6, line 16.

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Please delete the paragraph beginning on page 6, line 26.

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Please delete the paragraph beginning on page 7, line 8.

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Please delete the paragraph beginning on page 7, line 15.

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Please delete the paragraph beginning on page 8, line 1.

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Please delete the paragraph beginning on page 8, line 8.

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Please delete the paragraph beginning on page 8, line 16.

IN THE CLAIMS

✓
Please cancel Claim 4 without prejudice.

Please amend Claims 1-3 and 11-14 as shown in clean form below.²

A2
1. (Amended) A nonvolatile semiconductor memory device comprising:

M/ 2 A marked-up copy of the amended portion of the claims is attached hereto.